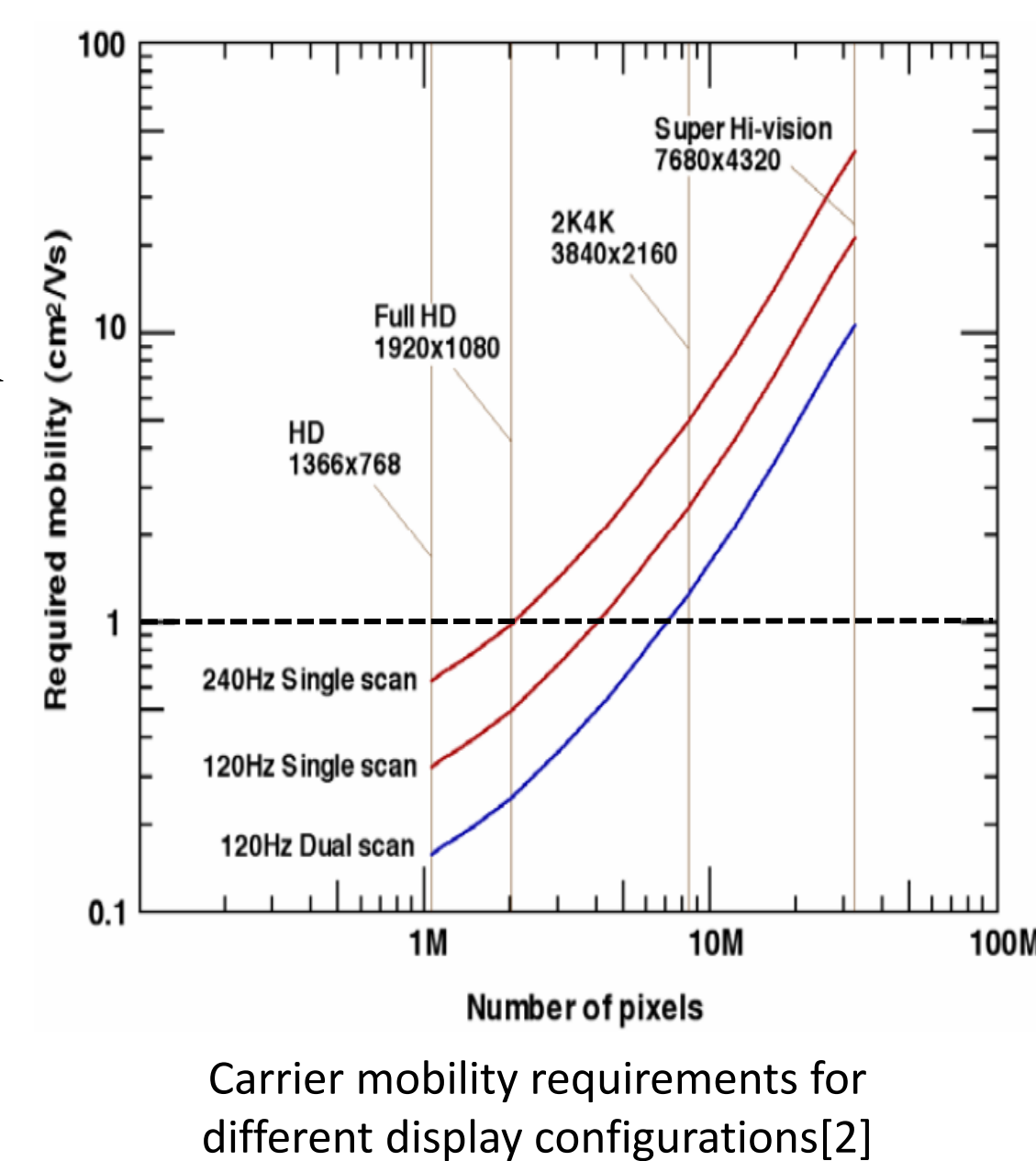
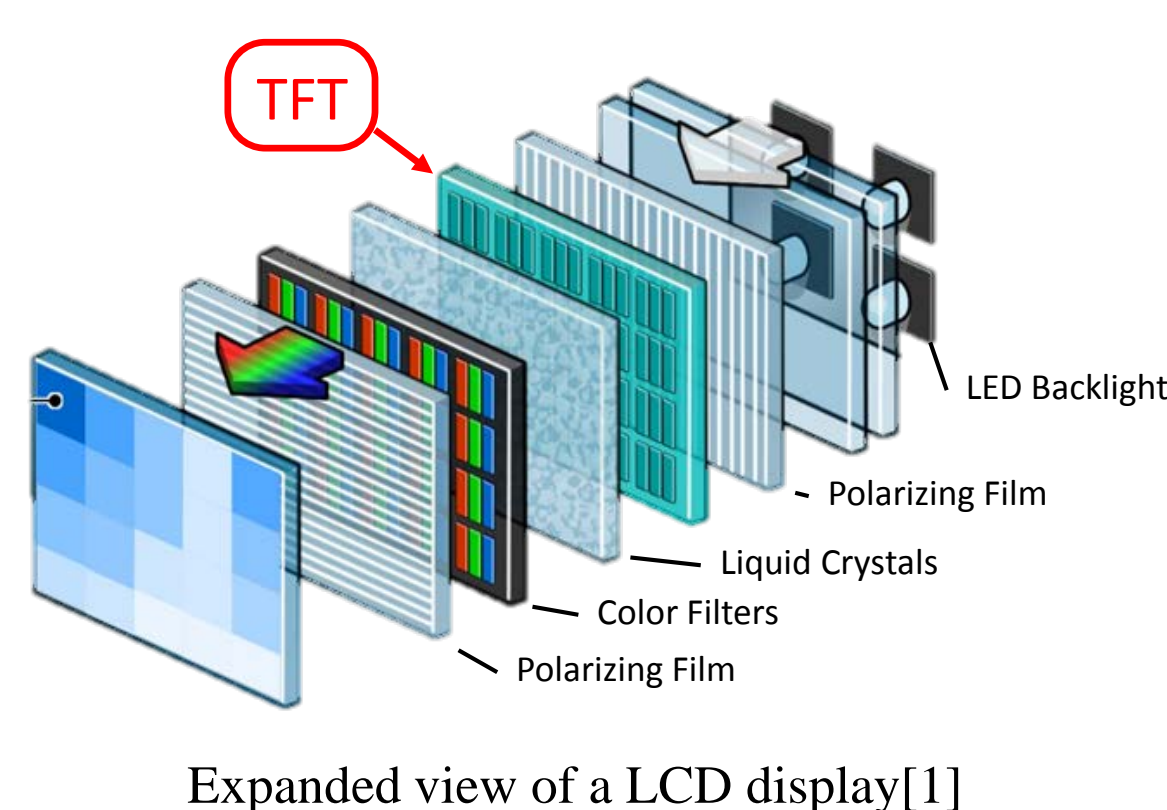


I. Project Objectives

- To investigate the addition of a fluorine implant to enhance the activation of boron in transistor source/drain regions during low temperature activation
- To develop a process that results in low resistance source/drain and is compatible with self-aligned CMOS thin film transistors

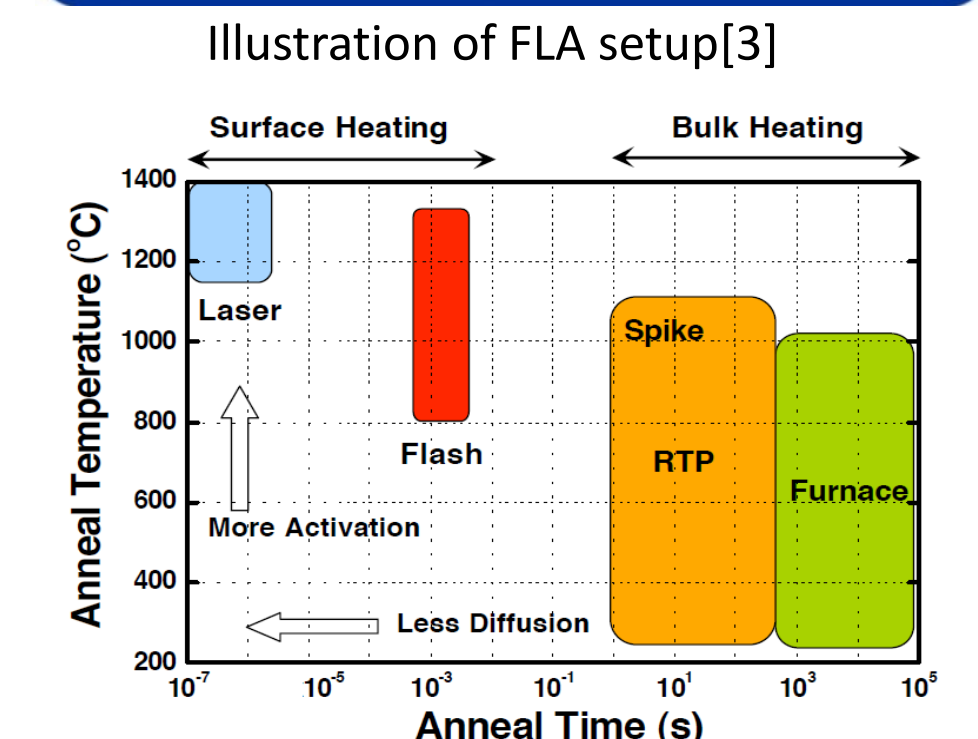
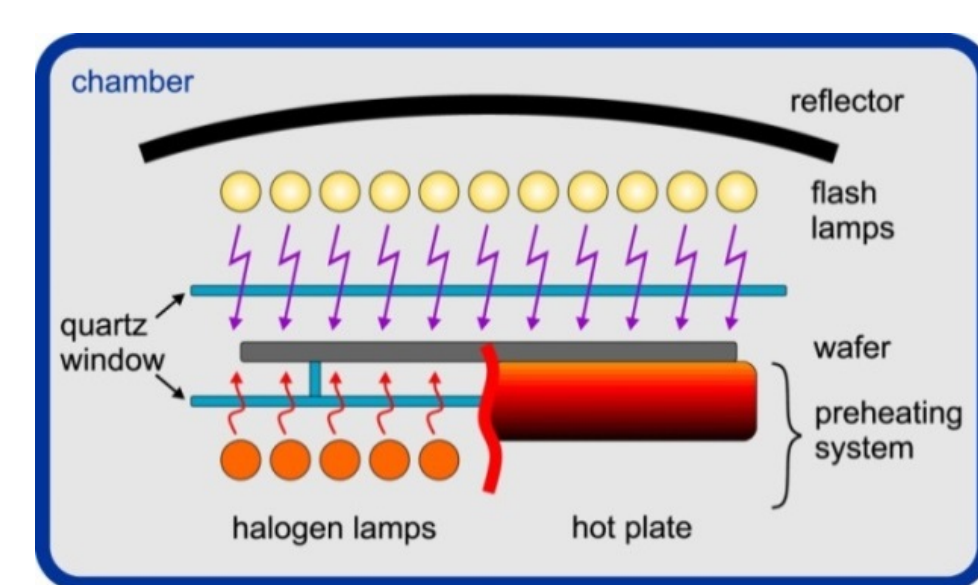
II. Motivation

- Thin film transistors (TFTs) are used in the backplanes of LED and OLED displays
- Currently, most TFTs are made of amorphous silicon (aSi:H)
- These devices are limited to NMOS, and have electron mobility less than $1 \text{ cm}^2/\text{Vs}$
- Next generation displays require TFTs made from higher mobility materials
- Devices fabricated using flash lamp annealed polysilicon (FLAPS) are CMOS, high mobility, scalable, and compatible with existing manufacturing
- CMOS TFTs allow for incorporation of external control circuitry to be incorporated onto display



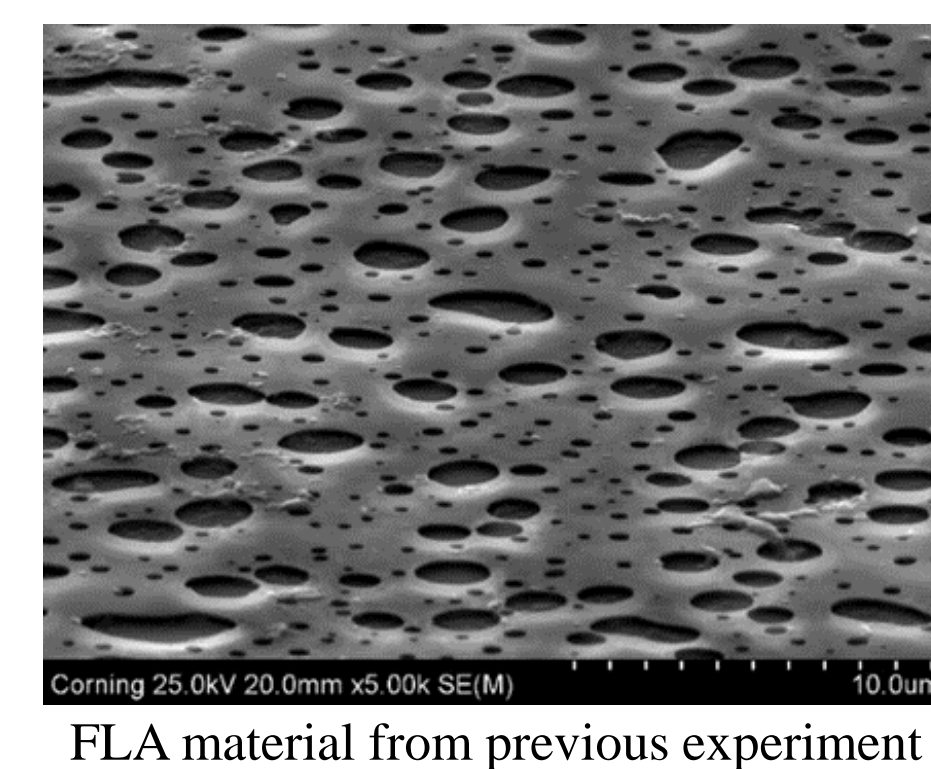
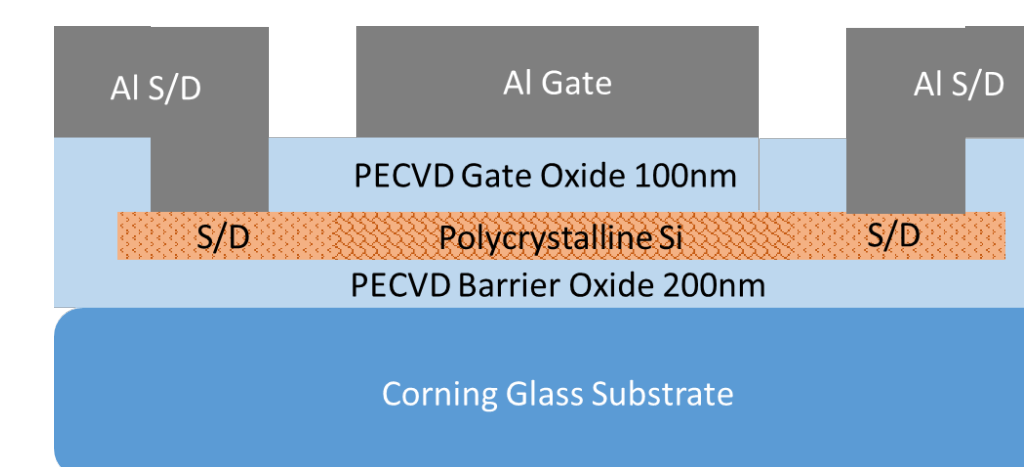
III. Overview of Flash Lamp Annealing

- Heated sample is exposed to a pulse of light from broad-spectrum Xe flashbulbs
- Si film absorbs light, rapidly heating and melting
- Glass substrate does not absorb light, staying below its thermal limit
- Si solidifies resulting in a polycrystalline film
- This flash lamp system is scalable allowing larger displays to be fabricated



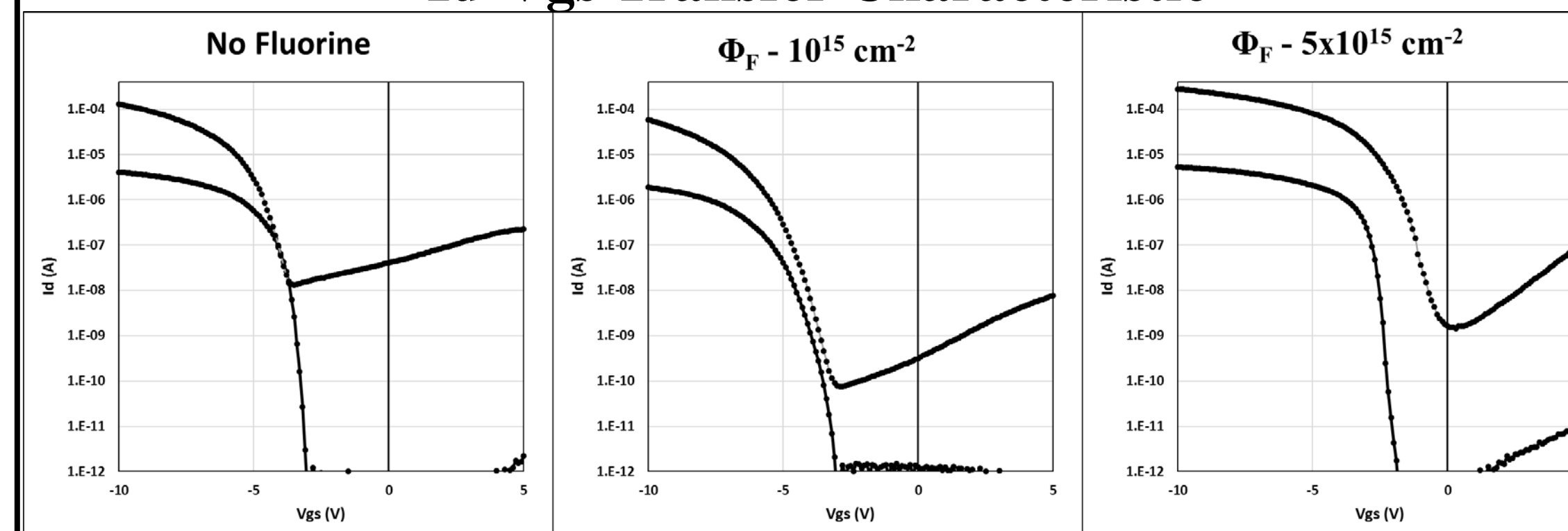
IV. Device Fabrication

- Devices were fabricated using a previously developed FLAPS TFT process
- Source/drain implant was performed after FLA; fluorine followed by boron
- Fluorine dose of 1×10^{15} and $5 \times 10^{15} \text{ cm}^{-2}$ were chosen
- Fluorine has shown to increase boron activation at low temperature (600°C) in crystalline silicon[4]
- Fabrication flow compatible with self-aligned devices



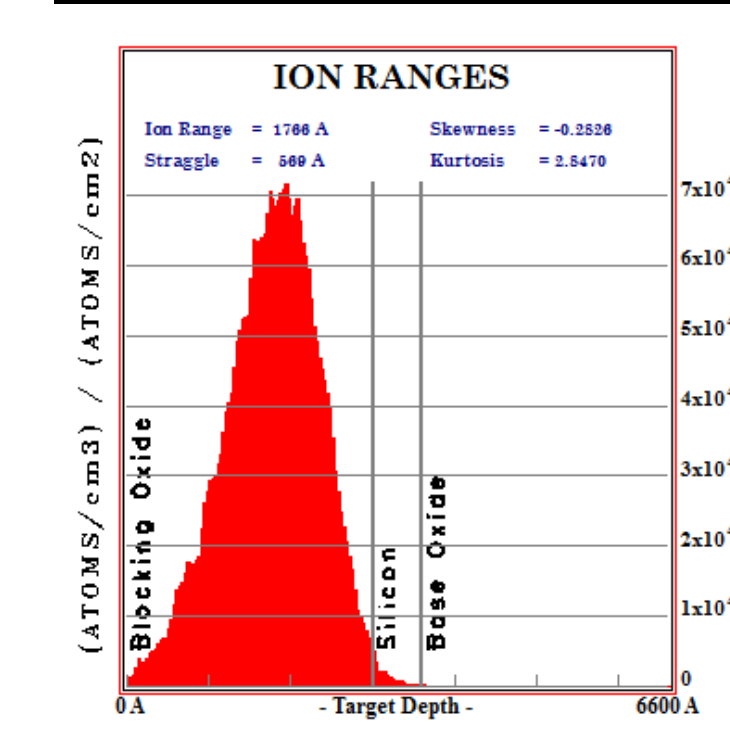
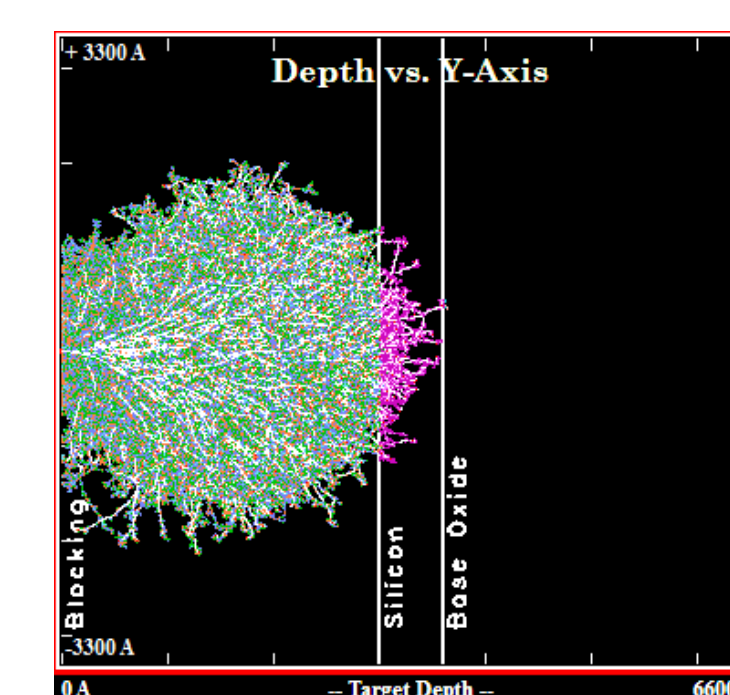
V. Results

Id-Vgs Transfer Characteristic



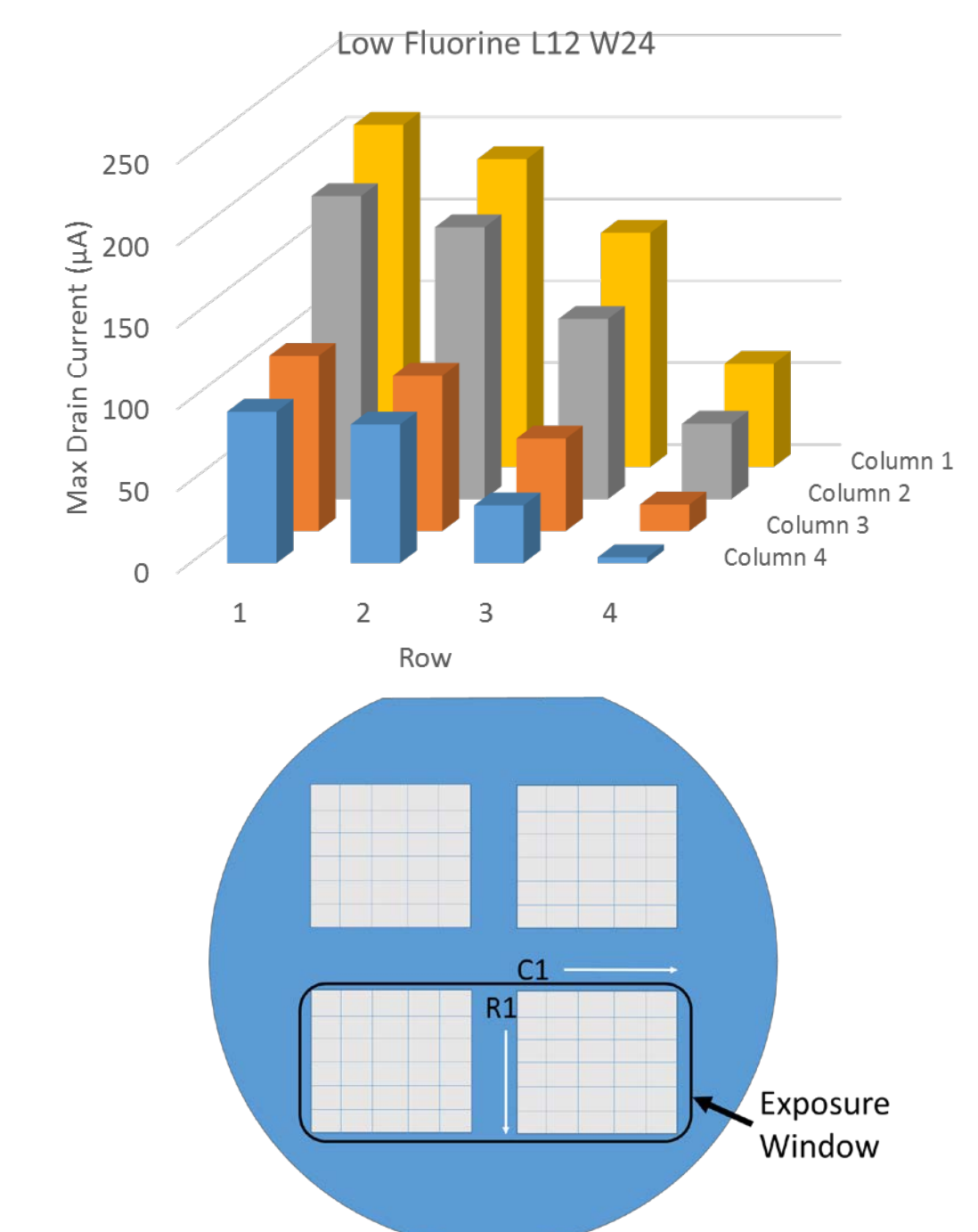
Fluorine Dose	None	10^{15} cm^{-2}	$5 \times 10^{15} \text{ cm}^{-2}$
Linear V_T	-3.5 V	-4 V	-2.4 V
ΔV_T	0 V	0.3 V	2 V
μ_{lin}	$24 \text{ cm}^2/\text{Vs}$	$13 \text{ cm}^2/\text{Vs}$	$28 \text{ cm}^2/\text{Vs}$
μ_{sat}	$140 \text{ cm}^2/\text{Vs}$	$70 \text{ cm}^2/\text{Vs}$	$220 \text{ cm}^2/\text{Vs}$
I_{Dmax}	$131 \mu\text{A}$	$58 \mu\text{A}$	$280 \mu\text{A}$

- High fluorine dose devices have increased current
- DIBL like effect occurring with the increase of fluorine
- These results suggest increased conductivity and decreased gate control
- SRIM simulations suggest fluorine penetration into channel region
- F+ associated defects may be responsible



VI. Location Dependence

- Device characteristics change consistently depending on location on wafer
- Most likely cause is variation in crystallinity due to non-uniform exposure condition
- Direct comparison between treatments is difficult
- Improved system control can mitigate this issue



VII. Conclusions

- Van der Pauw measurements inconsistent with transistor performance due to differences in the influence of grain boundaries
- Direct comparison on impact of fluorine on boron activation inconclusive due to a portion of the fluorine implant entering the channel
- Devices with high fluorine dose showed increased current, indicating a lower source/drain series resistance
- High dose devices have less gate control, high off state leakage and threshold voltage shift, indicative of a conductive pathway
- Study is currently being replicated with thicker blocking oxide
- Non-uniformity in the exposure window complicates direct device comparisons and statistical analysis

VIII. References

- <https://www.flatpanelshd.com/focus.php?subaction=showfull&id=1474618766>
- Y. Matsueda, "Required characteristics of TFTs for next generation flat panel display backplanes," *Digest of Int. Transistor Conf.*, p. 314, 2010.
- Prucnal, S., Rebohle, L. and Skorupa, W. (2017). Doping by flash lamp annealing. *Materials Science in Semiconductor Processing*, 62, pp.115-127.
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